

FIG. 2

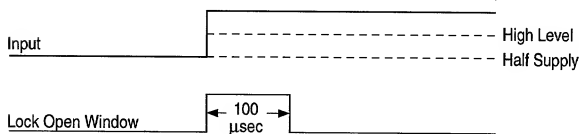


FIG. 3

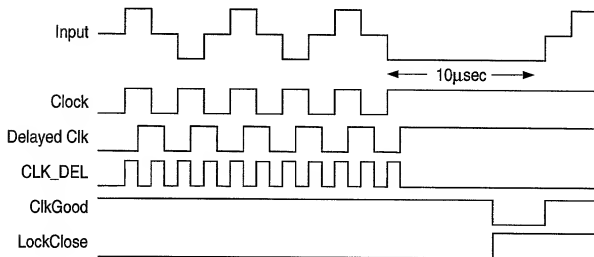


FIG. 4

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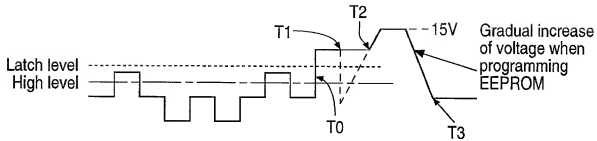


FIG. 5

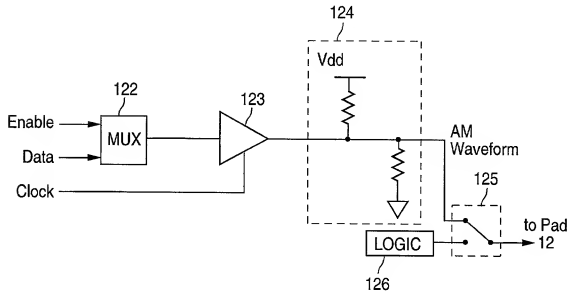


FIG. 6

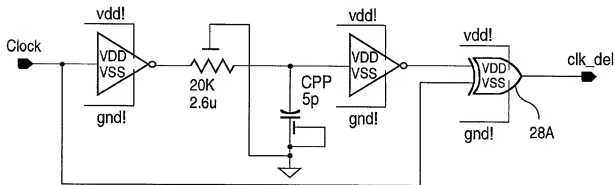


FIG. 9

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FIG. 7A	FIG. 7B
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FIG. 7A



FIG. 8A | FIG. 8B



FIG. 8B

The circuit diagram (FIG. 8B) illustrates a digital-to-analog converter. It features an SRFlipFlop (37) with inputs R, S, Q, and Qb. Node D is connected to the S input. The Q output is connected to the R input and the input of an inverter (INVX1_TA00). The Qb output is connected to the input of another inverter (INVX1_TA00). The circuit also includes a network of transistors (M108, M109, M115, M116), resistors (R111, R121), and a capacitor (C112). The output of the circuit is SDanalog. The timing diagram shows the relationship between Input, Vcap, SDanalog, DigLockRST, and ENDefSD over a 100µsec period.

In re Patent Application of
Jeffrey P. Kotowski, et al.
**INTEGRATED CIRCUIT AND METHOD FOR
TESTING SAME USING SINGLE PIN TO...**
Express Mail No.: EL 884994997 US
Attorney Docket No.: NSC1-G9800 [P05051]
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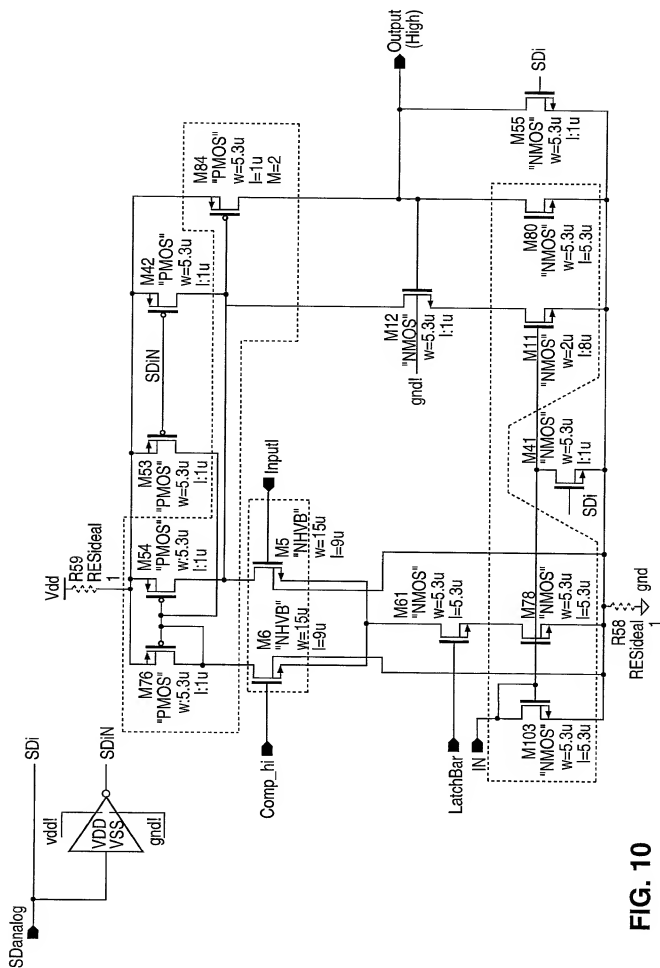


FIG. 10

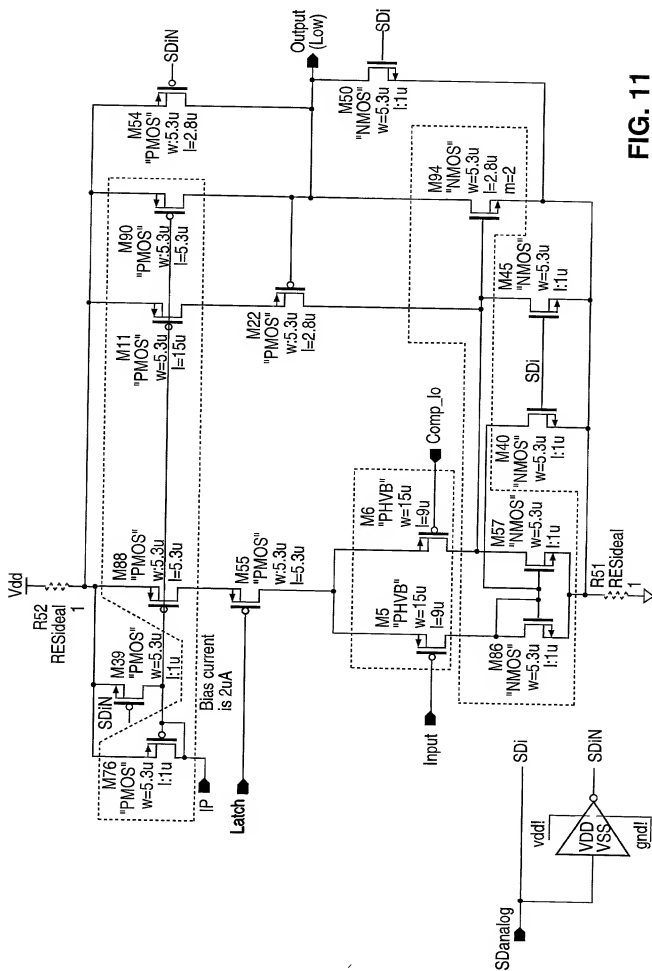
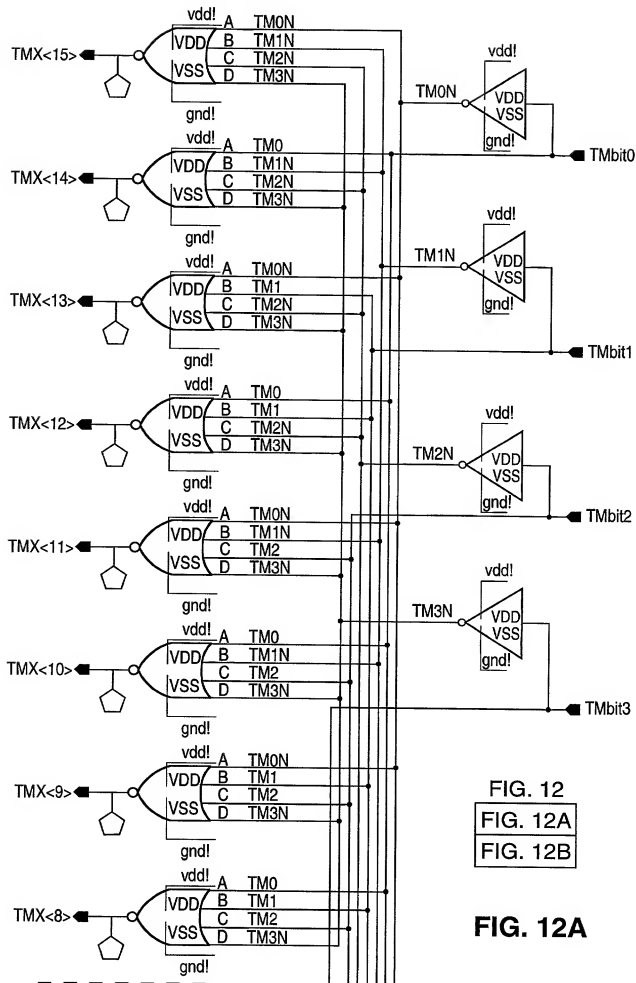
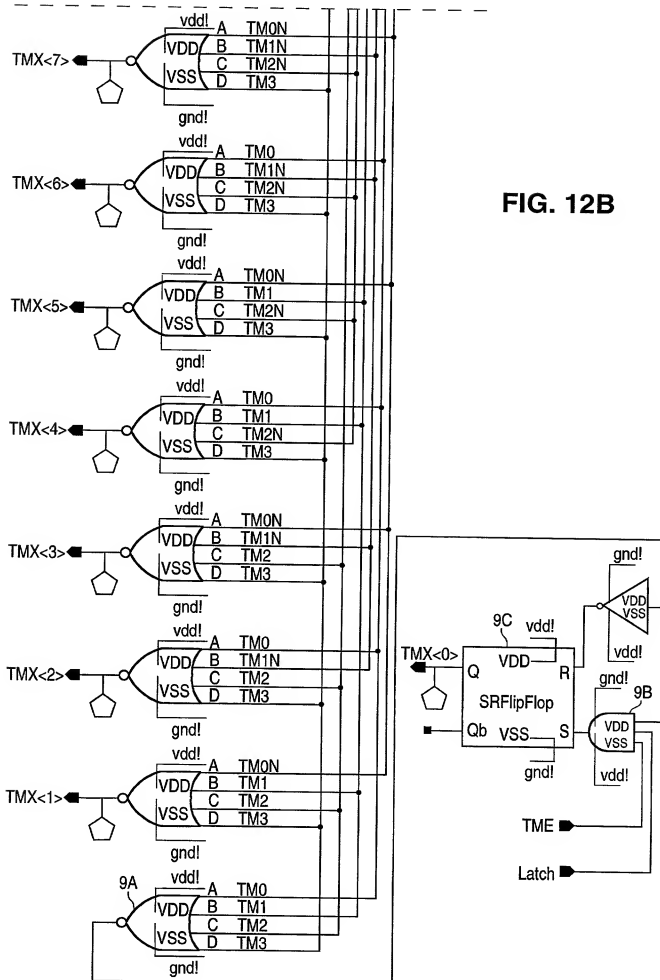


FIG. 11





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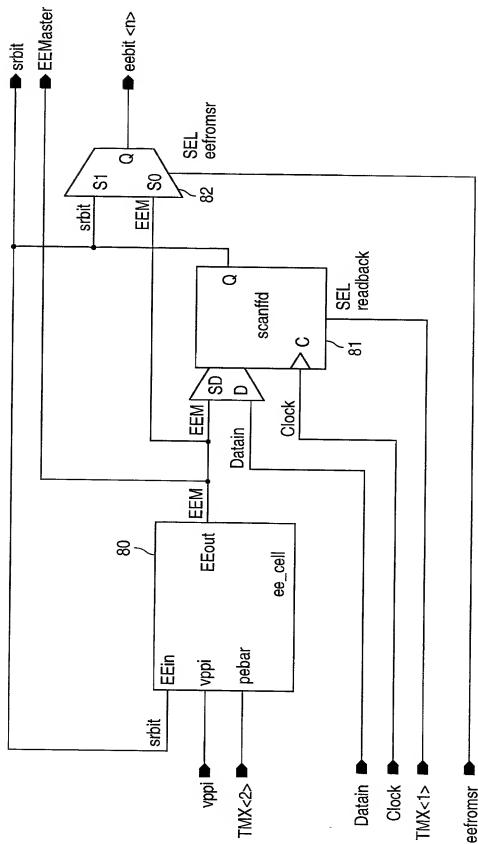


FIG. 13